

## CLAIMS

1. A balanced gyrator comprising a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced  
5 inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough capacitance of the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

10

2. A balanced gyrator as claimed in claim 1, wherein each of the single-ended transconductors comprises a pMOS transistor and a nMOS transistor having drain electrodes connected together, source electrodes connected to respective first and second power supply lines, gate electrodes  
15 coupled to an input, and a junction of the interconnected drain electrodes connected to an output, characterised in that the non-reciprocal feedback capacitance comprises a capacitive device coupled between the input and output.

20 3. A balanced gyrator as claimed in claim 2, characterised in that the capacitive device comprises a MOS transistor having its source and drain electrodes connected together and a gate electrode, in that the gate electrode is coupled to the transconductor input and in that a source follower transistor couples the interconnected source and drain electrodes to the transconductor  
25 output.

4. A balanced gyrator as claimed in claim 3, characterised in that the capacitance value of the capacitive device is related to the sum of the gate-source capacitances of the pMOS and nMOS transistors.

30

5. A balanced gyrator as claimed in claim 4, characterised in that the capacitance value is substantially equal to:  $\frac{2}{5}(C_{gsp} + C_{gsn})$ , where  $C_{gsp}$  and  $C_{gsn}$ , respectively are the gate-source capacitances of the pMOS and nMOS transistors.

5

6. A filter comprising at least one stage including first and second shunt capacitors and a series inductance stage, characterised in that the series inductance stage comprises first and second balanced gyrators and a shunt capacitance and in that each of the first and second gyrators comprises  
10 a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough capacitance of  
15 the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

7. A transceiver having at least one channel filter, the or each channel filter comprising a plurality of balanced gyrators, each balanced  
20 gyrator including a plurality of interconnected feedforward and feedback MOS single-ended transconductors, balanced inputs and outputs, common mode feedback means coupled respectively between the balanced inputs and outputs, and means for providing each of the transconductors with a non-reciprocal feedback capacitance for rendering reciprocal the feedthrough  
25 capacitance of the transconductor thereby neutralising the feedthrough capacitance of the gyrator.

8. A transceiver as claimed in claim 7, wherein each of the single-ended transconductors comprises a pMOS transistor and a nMOS transistor  
30 having drain electrodes connected together, source electrodes connected to respective first and second power supply lines, gate electrodes coupled to an

input, and a junction of the interconnected drain electrodes connected to an output, characterised in that the non-reciprocal feedback capacitance comprises a capacitive device coupled between the input and output.

5           9.     A transceiver as claimed in claim 8, characterised in that the capacitive device comprises a MOS transistor having its source and drain electrodes connected together and a gate electrode, in that the gate electrode is coupled to the transconductor input and in that a source follower transistor couples the interconnected source and drain electrodes to the transconductor  
10     output.

          10.    A transceiver as claimed in claim 8, characterised in that the capacitance value of the capacitive device is related to the sum of the gate-source capacitances of the pMOS and nMOS transistors.

15

          11.    An integrated circuit comprising a filter as claimed in claim 6.

          12.    An integrated circuit comprising a transceiver as claimed in any one of claims 7 to 10.

20